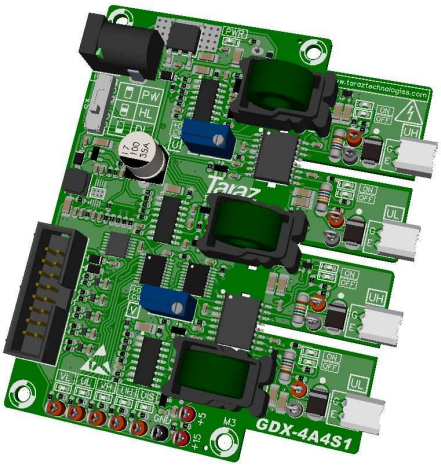
GDX-4A4S1

High CMR Isolated 4SW 4A Gate Drive Module For SiC FETs



Features

- Best Cost to Performance Ratio in the Market.
- Suitable for 1200V SiC FET, IGBTs & MOSFETs up-to 120A.
- 4A Peak Gate Drive Current.
- 3000 V_{RMS} Input to Output Isolation.
- Output UVLO Protection.
- Output Clamping Protection.
- Configurable Dead-Time.
- Configurable PWM/High-Low/Dual Inputs.
- 100KV/us Minimum Common Mode Rejection (CMR).
- 5MHz Max. Frequency Operation.
- Ultra-Low Propagation Delay of 30ns Max.
- 20ns Min. Pulse Width.
- Input & Output Indication LEDs for Visual Feedback.
- Input & Output Test points.
- Built-in 5V Regulator for Powering up External Control Circuitry.

Applications

- 4 Switch Isolated SiC/IGBT/MOSFET Gate Driver
- Full Bridge Drives
- DC-DC Converters
- Switched Mode Power Supplies
- Multi-Phase PFC Rectifiers

Compliance

- ROHS

Description

The GDX-4A4S1 is high performance fully isolated SiC/IGBT/MOSFET gate drive module for 4 Switches. It is specially designed for fastest inverter prototyping in research and educational environments. The drive use's Texas Instrument's UCC21520 high performance gate driver IC, and feature's dead time generation logic, input and output indication LEDs, test points and built in 5V regulator which could be used to power up external control circuitry.

But the most notable feature of this module is its ultra-low propagation delay of less than 30ns. This is particularly important for very high switching frequency applications such as ZVS and ZCS topologies, it's also ideal for cascaded and parallel topologies to minimize differences between switches. Overall, this module will achieve fastest gate drive operation and lowest output signal distortion. Another major feature of GDX series is very high common mode immunity of 100 kV/us. Due to very high switching speeds of SiC FETs, high immunity is required for proper operation of the gate driver module.

This product can be ordered with different output voltages suitable for different available SiC FETs in the market. Available options are +20/-5, +18/0, +15/0, +15/-5 & +15/-15.

Revision History Table

Version	Release Date	Changes
1.0	4/09/2019	First Version Released

WARNING AND DISCLAIMER !

ATTENTION PLEASE! THE INFORMATION HEREIN IS GIVEN TO DESCRIBE CERTAIN COMPONENTS AND SHALL NOT BE CONSIDERED AS A GUARANTEE OF CHARACTERISTICS. TERMS OF DELIVERY AND RIGHTS TO TECHNICAL CHANGE RESERVED. WE HEREBY DISCLAIM ANY AND ALL WARRANTIES, INCLUDING BUT NOT LIMITED TO WARRANTIES OF NON-INFRINGEMENT, REGARDING CIRCUITS, DESCRIPTIONS AND CHARTS STATED HEREIN. CUSTOMER IS SOLELY RESPONSIBLE OF PROPER AND LEGAL USE OF ALL PRODUCTS OFFERED BY TARAZ TECHNOLOGIES.

SAFETY NOTICE !

ATTENTION PLEASE! THIS DEVICE IS ESD SENSITIVE AND NEEDS TO BE HANDLED WITH CARE. HIGH VOLTAGE CONDITION MAY OCCUR DURING OPERATION OF THE DEVICE, AND HENCE USER IS SOLELY RESPONSIBLE OF EQUIPMENT AND PERSONNEL SAFETY. TARAZ TECHNOLOGIES SHALL NOT BE HOLD LIABLE FOR ANY DAMAGE TO PERSONNEL AND/OR PROPERTIES AS A RESULT OF USING THIS DEVICE. USER MUST TAKE ADEQUATE STEPS TO ENSURE ELECTRICAL AND MECHANICAL SAFETLY OF THE DEVICE IN USE.

Table of Contents

Ratings & Characteristics

*All ratings are given at Vs=15V and 25°C ambient temperature unless otherwise specified.

Absolute Maximum Ratings	Test Conditions/ Note	Value	Unit
Supply Voltage (V_S)		18	V
Input Signal Voltage HIGH		5.5	V
Input Signal Voltage LOW		0	V
Output Peak Current ($I_{out(PEAK)}$)	Using Rg<10Ω	4	A
Output Power (P_{out})	Per Channel	0.5	W
Maximum Working Insulation Voltage	Vpeak	1200	V
Input to Output Isolation	AC RMS	3000	V
J1 5V Output Current (I_{OUT5V})	Supply for external circuit	180	mA
Operating Temperature	I_{OUT5V} = 0	-25 to +70	°C
Storage Temperature		-25 to +85	°C

Recommended Operating Conditions	Test Conditions/ Note	Minimum	Typical	Max	Unit
Supply Voltage (Vs)		13	15	17	V
Supply Current			100	300	mA
Operating temperature	I_{OUT5V} = 0	-10	-	70	°C
Input Signal Voltage On/Off	3.3V control signals possible		5/0		V

Ratings & Characteristics (Continued)

*All ratings are given at Vs=15V and 25°C ambient temperature unless otherwise specified.

Characteristics	Test Conditions/ Note	Minimum	Typical	Max	Unit
Logic High Input Threshold		2.0	-	-	V
Logic Low Input Threshold		-	-	0.8	V
Output Voltage (+20/-5 option)	V_S = 15V, 20mA $I_{out(AVG)}$	-5		20	V
Output Voltage (+18/0 option)	V_S = 15V, 20mA $I_{out(AVG)}$	0		18	V
Output Voltage (+15/0 option)	V_S = 15V, 20mA $I_{out(AVG)}$	0		15	V
Output Voltage (+15/-5 option)	V_S = 15V, 20mA $I_{out(AVG)}$	-5		15	V
Output Voltage (+15/-15 option)	V_S = 15V, 20mA $I_{out(AVG)}$	-15		15	V
Output UVLO Threshold	UVLO + UVLO -	5.7 5.4		6.3 6	V
Output Clamp Threshold	Of Bi-directional TVS @ 1mA	22.2	-	24.5	V
Fault Output Voltage	Active LOW	-	-	0.8	V
Input Impedance	All inputs have 22 kΩ pull-down resistors	-	22	-	kΩ
Internal Gate to Emitter Resistance		-	6.2	-	kΩ
Duty Cycle Range		0	-	100	%
Configurable Dead-time	Using DT-ADJ	5	-	5000	ns
Propagation Delay		14	19	30	ns
Output Rise and Fall Time	C_g = 1.8nF	-	7	16	ns
Minimum Pulse Width		-	20	-	ns
Maximum Frequency		-	-	5	MHz
Common Mode Rejection (CMR)	At V_{CM}=1500V	100	-	-	kV/us
Weight		-	46	-	g
Dimensions (Bare)	Width x Length x Depth		74x91.44x 21.68		mm

Block Diagram

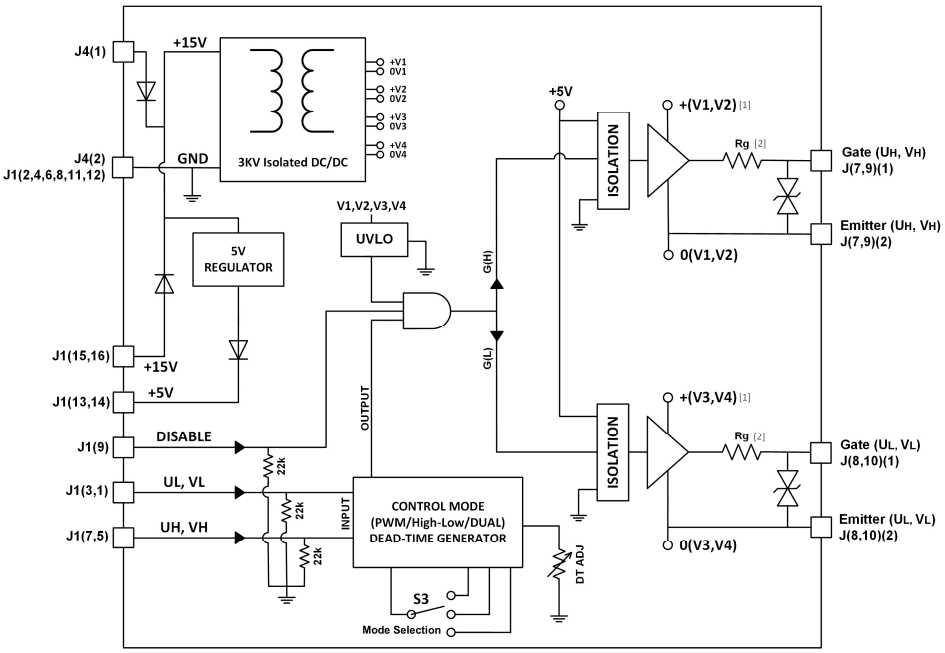
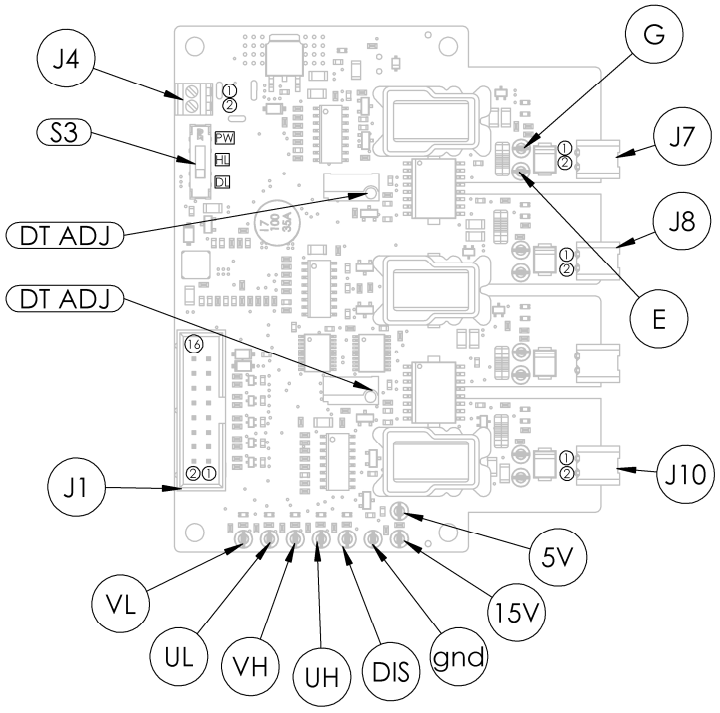


Figure 1: Block Diagram

Notes:

1) All drivers are powered by isolated (floating) voltage sources.
2) The default gate resistor is 10Ω and user can control the gate turn on and off by changing Rg to lower value for faster switching, or higher value to minimize ringing. However, the minimum value to be used should be greater than or equal to SiC/IGBT/MOSFET datasheet recommended value for reliable operation.
3) In case of PWM mode, control signals will be generated from UH and VH. User don't have to supply the UL and VL signals.

Pin Description



Name	Connector (Pin No.)	Description
UH, VH	J1(7,5)	Non-inverting logic input terminal for HIGH side gate.
UL, VL	J1(3,1)	Non-inverting logic input terminal for LOW side gate.
GND	J4(2), J1(2,4,6,8,11,12)	Ground
+15V	J4(1), J1(15,16)	+15V supply voltage (Vs) for the module. It can be supplied either from J4 or J1.
+5V	J1(13,14)	+5V supply output from the module to power up the external circuit.
DISABLE	J1(9)	Input disable signal, active high will drive all outputs to LOW.
Gate	J(7,8,9,10)(1)	Output to SiC/IGBT/MOSFET gate terminal.
Emitter	J(7,8,9,10)(2)	Output to SiC/IGBT/MOSFET emitter terminal.
PWM / High-Low / Dual	S3	Operation mode can be selected using S3, in PWM mode, user have to input UH & VH signals where UL & VL signals are internally generated, in High-Low mode, user have to supply all signals, but the module will insure no overlapping and appropriate dead time is inserted. In Dual mode, user have to supply all signals and all drivers will work independently.
Dead-Time Adjust	DT-ADJ	Duration of Dead-time can be adjusted by DT-ADJ potentiometer.

Application Information

Typical Application Circuit

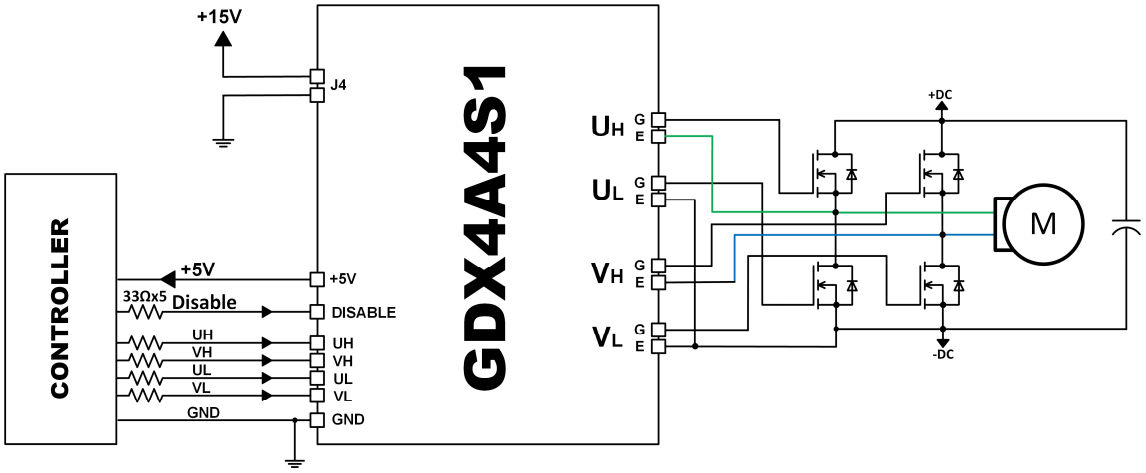


Figure 2: Typical application circuit

Operation Requirements

For proper operation of the gate drive module, certain requirements need to be fulfilled. First, the module need to be supplied with +15V voltage source through J4 or J1 connectors. In addition, control signals need to be given to the module with recommended 33 Ohm transmission resistors to avoid ringing and noise. Last, Disable signal must be in low state.

Power Supply & Configuration (J1 & J4)

Supply voltage (+15V) is provided through J4 terminal block. It can also be supplied from J1 (pins 15,16). Moreover, user can utilize 5V supply from J1 (pins 13,14) to power external control circuit.

Output Connection (J7-J10)

Output connectors from J7 to J10 should be directly connected to power switches accordingly. Gate and emitter wires are recommended to be in twisted pairs in case of free hanging connectors and must be as short as possible.

Operation Modes (S3)

User can select to use this gate driver as High/Low (HL), PWM (PW) or Dual (DL) input mode using S3. All gate driver modules are pre-configured in PWM mode by default. In PWM mode, user have to input UH and VH signals, while UL and VL signals are internally generated by dead-time generation logic, in High-Low mode, user have to supply all signals, but the module will insure no overlapping occurs and appropriate dead time is inserted between output pairs. In Dual mode, all channels are independently controlled through respective signals, this is required for some topologies where shoot-through is needed such as Z-Source Inverter.

Application Information (Continued)

Configurable Dead Time (DT ADJ) in PWM Mode

User can configure the internal dead time using DT ADJ potentiometer. The duration of dead time delay DT can be calculated as per equation 1.

$$DT \approx 10\ x\ RDT$$

Equation 1.

Where: DT= dead time (ns), and RDT= on board dead time programming trimmer (kΩ), which varies from 0.51k to 500kΩ, changing dead time from 5ns to 5µs. By default, the module is configured at 500ns dead time. If dead time need to be adjusted, it must be done with switches high voltage power supply in OFF condition.

Selecting Appropriate Output Voltage for SiC Devices

Due to variety of available SiC devices in the market, gate drive voltage requirements of each SiC device varies greatly, choosing the correct voltage is important for reliable operation of the switch and gate driver. Following are examples of different series SiC devices with recommended gate drive voltages.

SiC Series	Manufacturer	Output Voltage	Also Use for
C3M	Cree	+15V/-5V	IGBTs & MOSFETs
C2M	Cree	+20V/-5V	
SCT	Rohm	+18V/0V	

Input & Output Indication LEDs, Test Points

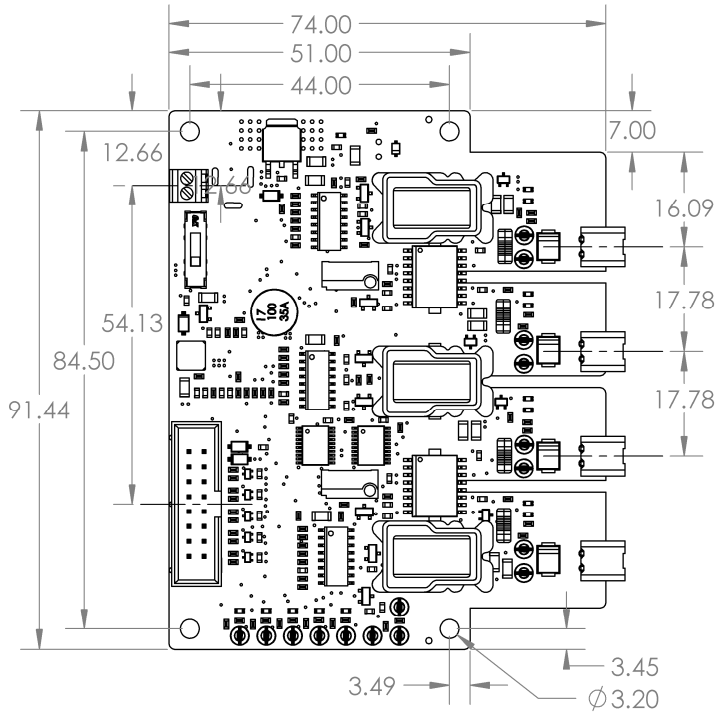
LEDs are provided on input and output signals for instant user feedback. Input side LEDs are yellow colored. While output LEDs are independent for ON (Orange) state and OFF (Yellow) state so user can have feedback of high frequency PWM signals as well. Separate LEDs also indicate DISABLE (Orange) and Power state (Green).

The module also has input and output test points for easy debugging. This is very helpful feature for educational and research use. Test points are available on all inputs, Disable, Power (+15V, +5V, GND) and Gate, Emitter of all outputs.

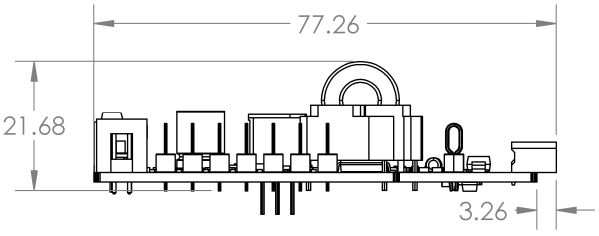
Mounting and Safety

Since output side may carry dangerous high voltage, it is not safe to touch the circuit in operation. User must consider proper clearance of heat sink, metal enclosure, stray metallic objects near output side, and cover module and inverter with proper insulated casing. Care must be taken with mounting since mounting holes are close to outputs.

Mechanical Drawing



TOP VIEW



SIDE VIEW

Notes:

* All dimensions are in mm.

Ordering Information

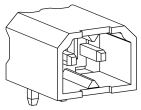
GDX - 4A 4S 1 - XXX - XX

- **GDC**-Xtreme Series
- Gate Current *in Ampere*
- Number of Switches
- Version
- Output Voltage
  - **205** -*20/-5V*
  - **180** -*18/0V*
  - **150** -*15/0V*
  - **155** -*15/-5V*
  - **151** -*15/-15V*
- Rg=
  - *10*Ω
  - *22*Ω
  - *47*Ω

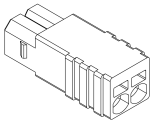
Notes:

1) The default gate resistor is 10Ω. However, user can control gate turn on and off speed by changing Rg to a lower value for faster switching or higher value to minimize ringing effect. The minimum value to be used should be greater than or equal to SiC/IGBT/MOSFET datasheet recommended value for reliable operation.

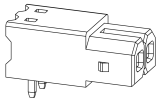
Output Connectors



Output Connector (PCB):
1814841



Plug (Wire to Plug):
1704853



Plug (PCB to PCB): Not Supplied
1814980

For Further information or purchasing, please go to our web site:
www.taraztechnologies.com
Address: 21-X, 2nd Floor, DHA Business Avenue, DHA Phase 1, Bahria Expressway, Rawalpindi 46000, Pakistan
Phone: +92 (51) 5400335
Fax: +92 (51) 5400155
E-Mail: info@taraztechnologies.com

Think Beautifully®
Taraz
TECHNOLOGIES